



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#30

Applicant: Hiroyuki Enomoto, et al.
Serial No.: 09/019,087
Filed: 02/05/98
For: Manufacturing Method of
Semiconductor IC Device

Docket No.: TIJ-24816
Art Unit: 1765
Examiner: Perez Ramos, V
Confirm. No.: 1640

APPEAL BRIEF TRANSMITTAL FORM

Assistant Commissioner For Patents
Washington, DC 20231

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William B. Kempler

Date

Sir:

Transmitted herewith in triplicate is an Appeal Brief in connection with the above-identified application.

Please charge \$320.00 fee for filing the Brief to Deposit Account No. 20-0668.

To the extent necessary, the Applicants petition for an Extension of Time under 37 CFR 1.136. Please charge any additional fees in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

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APPEAL BRIEF

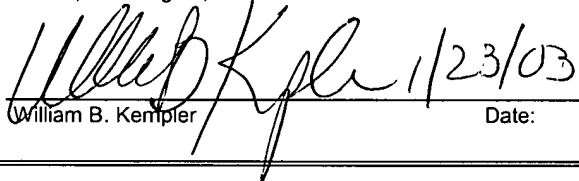
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William B. Kempler Date: 1/23/03

The following Appeal Brief is respectfully submitted in support of an appeal of the final rejection of Claims 1-11 in connection with the above-identified application. The final Rejection was mailed on 07/23/2002, and the Advisory Action mailed 10/10/2002 and the Notice of Appeal was received by the Office on 10/29/2002.

REAL PARTY IN INTEREST

The invention has been assigned to Texas Instruments Incorporated and Hitachi LTD.

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RELATED APPEALS AND INTERFERENCES

There are no appeals or interferences known to Applicant's representative which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

STATUS OF THE CLAIMS

Claims 1-10 stand rejected. The Application was filed on 02/05/1998 with 5 claims and amended on filing by a Preliminary Amendment which added Claims 6-11. Claims 1-3 were amended 09/10/1999, 07/11/2201, and 01/10/2002. All claims 1-11 were rejected in the final rejection of 07/23/2002. Claim 11 is being cancelled herewith.

STATUS OF THE AMENDMENTS

In response to the final rejection of 07/23/2002, Applicants requested a reconsideration and did not make amendments to the claims. Applicant has submitted herewith an amendment canceling Claim 11, which has not been entered.

SUMMARY OF THE INVENTION

The present invention is related to a manufacturing method for manufacturing integrated circuits and more specifically to the formation of connecting holes and trenches (page 2, line 17-19).

In the present invention, a hook-shaped hard mask is formed from a first and second mask film and used to etch the connecting hole or trench. In a first embodiment of the invention, a thin polysilicon film (first mask film) 3 is formed on a silica (insulating) film 2 using the CVD method. A resist film 4 is coated on the semiconductor substrate and

patterned for forming the trenches by photolithographic technology. Using the resist 4 as an etching mask, polysilicon film 3 is etched by means, for example, a microwave dry etching device. The outer layer of the silica film 2 below it is then etched by a parallel plate type of RIE (Reactive Ion Etching) device, to form trenches 2a in the region. The depth of the trenches 2a is larger than the thickness of the polysilicon film. After removal of the undesired resist film 4, a second polysilicon film (second mask film) 5 is formed on the semiconductor substrate using the CVD method, with the side surfaces of trenches 2a being covered with the polysilicon film. A dry etching or other selected etching method is utilized to remove at least the polysilicon film 5 below trenches 2a while the polysilicon film on the sidewall 5a remains. Polysilicon film 3 (first mask film) and polysilicon film 5 (second mask film) are then utilized as a hook-shaped hard etching mask in a dry etching or other selected etching process performed to form opening 2b on silica film 2, followed by the formation of trenches 1a on the semiconductor substrate 1 below it. During the silicon etching operation for forming the trenches 1a, polysilicon films 3 and 5a are etched off. In this process, even when the shoulder of the hook-shaped hard mask (the joint between polysilicon film 3 and polysilicon film 5a) is etched back due to abnormal etching conditions when silica film 2 is etched, because there is a vertical portion of the hook-shaped hard mask in the form of polysilicon film 5a on the sidewalls of trenches 2a, there is no change in the dimensions of the pattern of opening 2b and trenches 1a. Consequently, it is possible to form the fine structure opening 2b and trenches 1a with high dimensional precision. Furthermore, it is possible to etch and form the side surfaces of opening 2b and trenches 1a in the vertical direction which the pattern dimension of the hook-shaped hard mask are maintained. Consequently, even when the trenches 1a are deep, it is still possible to form trenches 1a with processing dimensions finer than the processing limit in conventional technology (page 10, line 15 through page 12, line 34 and figures 1-5).

In another aspect of the invention, in order to form an electrical connection between the lower electrode of capacitors in the COB (capacitor-over-bit line) type memory cells in a DRAM and plug 14 on semiconductor region 12 as the drain of the MOSFET formed on the semiconductor substrate 1, a thick silica film 17 is formed using CVD method on the surface of the semiconductor 1. A thin polysilicon film (first mask film) 18 is formed by the CVD method on the silica film 17. After resist film 19 is coated onto the semiconductor

substrate 1, lithographic technology is used to produce a pattern for forming the connecting holes on the resist film 19. After etching off polysilicon film 18 in the lower portion of the opening formed on resist film 19, using a resist film 19 as an etching mask, the outer layer of silica film 17 below the polysilicon film is etched, with trenches 17a being formed in this area having a depth greater than the thickness of the polysilicon film. After removal of the resist film 19, a second thin polysilicon film (second mask film) 20 is formed on the semiconductor substrate 1 using the CVD method and the side surfaces of trenches 17a are covered with polysilicon film 20. At least the polysilicon film 20 below trenches 17a is removed using dry etching or another selective etching method, while the polysilicon film 20a is left on the sidewalls of the opening and the sidewalls of the trenches 17a. Polysilicon film 18 (first mask film) and polysilicon film 20a (second mask film) are used as a hook-shaped hard mask to perform a dry etching over other selected etching operation to form connecting holes 21 on silica film 17 and silica film 15 (page 14, line 4 through page 15, line 16 and page 16, line 3 through page 17, line 2 and figures 10-14).

In another aspect of the invention, the upper electrode (plate electrode) 25 of a COB memory cell is connected to wiring utilizing the present invention. After the upper electrode 25 of the capacitor is formed, a thick silica film 26 is formed over the upper electrode 25 using the CVD method and a thin polysilicon film (first mask film) 27 is formed using the CVD method on the silica film 26. A resist film 28 is coated onto film 27 and photolithographic technology is used to pattern the resist film 28 to form trenches. After etching off the polysilicon film 27 in the lower portion of the opening formed on resist film 28, using resist film 28 as an etching mask, the outer layer of silica film 26 below the polysilicon film is etched, with trenches 26a being formed. The depth of the trench at 26a is greater than the depth of the polysilicon film. After removal of the undesired resist film 28, a thin polysilicon film (second mask film) 29 is formed on the substrate using the CVD method and the side surfaces of trenches 26a are covered with polysilicon film 29. At least the polysilicon film 29 below trenches 26a is removed using the dry etching or other selective etching methods, while polysilicon film 29a is left on the sidewall of polysilicon film 27 of the opening and of the sidewalls of the trenches 26a. Polysilicon film 27 and polysilicon film 29a are utilized as a hook-shaped hard mask in a dry etching or another selective etching operation to form trenches 30 on silica film 26. Undesired polysilicon film

27 and polysilicon film 29a are removed making it possible to bury a wiring layer in trenches 30 formed on silica film 26 (page 17, line 3 through page 19, line 7 and page 19, line 22, page 20, line 9 and figures 16-22).

Another aspect of the invention is utilized to form an electrical connection between the lower electrode 23 of a capacitor in the COD type memory cell of a DRM and a plug 14 on the semiconductor region 12 as the drain of a MOSFET formed on the semiconductor substrate by forming a connecting hole 21 on the insulating films 15 and 17, followed by the formation of plug 22 in connecting hole 21. In this case, polysilicon film 18 functions as the first mask film and polysilicon film 20a functions as the second mask film of a hook-shaped hard mask, with polysilicon film 20a being present on the sidewall of the trenches 17a on silica film 17 forming connecting holes 21 (page 20, line 19 through page 21, line 25 and figures 10-15).

In accordance with another aspect of the invention, an element-separating insulating film made of silica 6a is buried in trenches 1a. In this case polysilicon film 3 (first mask film) and polysilicon film 5a (second mask film) function as a hook-shaped hard mask with polysilicon 5a present on the sidewalls of trenches 2a on silica film 2 forming connecting-type openings 2b and trenches 1a (page 21, line 26 through page 22, line 26 and figures 1-5).

According to another aspect of the invention, a wiring layer 31a is formed flush with the surface of silica film 26. In this case, polysilicon film 27 (first mask film) and polysilicon film 29a (second mask film) functions as a hook-shaped hard mask, with polysilicon film 29a being present on the sidewalls of trenches 26a on silica film 26 forming trenches 30 (page 22, line 27 through page 23, line 25, and figures 17-20).

With regard to the claims, Claim 1 is described at page 14, line 11 through page 20, line 14 and in Figures 10-15. The insulating film is reference numeral 17 and semiconductor substrate is reference numeral 1. The first mask film is referenced numeral 18 and the resist film is reference numeral 19. The trenches are reference numeral 17a and the second mask film is reference numeral 20. The step of removing the second mask film from the bottom of the trenches while leaving the mask film on the sidewalls of the trenches is shown in Figure 12 and the step of using the first mask film and the second

mask film as an etching mask etching the trenches deeper to form connecting holes is shown in Figure 14.

Claim 2 is described at page 10, line 11 through page 13, line 3 and Figures 1-6. The insulating film is reference numeral 2 and the substrate is reference numeral 1. The first mask film is reference numeral 3 and resist film is reference numeral 4. The trenches are reference numeral 2a and the second mask film is reference numeral 5. The step in removing the second mask film from the bottom of the trenches while leaving it on the sidewalls of the trenches is shown in Figures 3 and 4. The step of using the first mask film and second mask film as an etching mask to etch the trenches deeper is shown in Figure 5. The step in burying an insulating film separating trenches to form a separating portion is shown in Figure 6.

Claim 3 is described in the application at page 17, line 35 through page 20, line 9 and Figures 17-22. The insulating film is reference numeral 26 and the substrate is reference numeral 1. The first mask film is reference numeral 27 and the first resist film is reference numeral 28. The trenches of reference numeral 26a and the second mask film is reference numeral 29. The step of removing the second mask film from the bottom of the trenches while leaving mask film on the sidewalls is shown in Figure 20. The step of using the first mask film on the second mask film as an etching mask in etching the trenches deeper is shown in Figures 21 and 22.

Claims 4, 7 and 9 are supported by the application at page 14, line 18-26. Claims 5, 6, 8 and 10 are support by the application at page 20, line 19 through page 21, line 25.

ISSUES

The single issue in this appeal is whether Claims 1-10 are unpatentable over Tsuji, U.S. Patent 5, 514,625 in view of Harari, U.S. Patent 4,933,739.

GROUPING OF THE CLAIMS

Each of the following groups of claims, as contained in the attached Appendix, are independently patentable, and the rejected claims of these groups stand or fall together for the reasons more clearly set forth hereinbelow:

Group I Claims 1, 4, 5, 6

Group II Claims 2, 7, 8

Group III Claims 3, 9, 10

Group I contains Claims 1, 4, 5 and 6 which stand or fall together.

Group II contains Claims 2, 7, 8 which stand or fall together. Claim 2 does not recite the formation of connecting holes, recited in Claim 1, but recites the formation of separating trenches on the semiconductor substrate and burying insulating film in the separating trenches to form a separating portion. Thus, Claim 2 is separately patentable from Claim 1 and the claims of group I.

Group III contains Claims 3, 9 and 10 which stand or fall together. Claim 3 does not recite the formation of connecting holes of Claim 1 or of a separating trench containing insulating film of Claim 2. Claim 3 recites the formation of wiring-forming trenches on the insulating film and burying an electroconductive material in the wiring-forming trenches to form a wiring layer. Therefore, Claim 3, and group claims of group III are separately patentable.

ARGUMENTS

The Examiner maintains her rejection of Claims 1-11 under 35 U.S.C. § 103(a) as being unpatentable over Tsuji in view of Harari. The Examiner's interpretation of Tsuji is incorrect as will be clear from the following. The Examiner states that Tsuji teaches a

method of manufacturing a semiconductor device comprising forming an insulating film over a substrate and refers to col. 5, lines 7-10. The embodiment described is shown in Figs. 2a and 2b of the patent. On lines 7-10, a substrate layer 19 is referred to as an insulating film and thus must be the film referred to by the Examiner. The Examiner states that a first mask film is formed on this insulating film and specifically refers to col. 5, line 24. Lines 24-25 recite "...the resist layer 22 is exposed to light, with the aid of a pattern as a first mask 23,...". Accordingly, the layer 23, shown in Fig. 2b, is to be formed on the insulating layer 19. Looking at the drawing, however, shows that layer 19 is at the bottom of Fig. 2b and that there are three intervening layers on the substrate: 20, 21, and 22 as well as an air space (unlabeled) before reaching element 23. That is because element 23 is a reticule, as is well known to those skilled in the art, which is utilized by the stepper to expose the resist layer 22 to the light shown impinging upon the reticule 23 in Fig. 2b.

Even if the Examiner meant that the insulating film is the interlayer insulating film 21, not recited until line 13, the Examiner's argument would still be incorrect because it still would require element 23 to be a mask film on the substrate. Column 5, lines 22-25 of Tsuiji recites in pertinent part "with use of the g ray stepper (not shown) for the first exposure, the resist layer 22 is exposed to light, with the aid of a pattern as a first mask 23, ..." Those skilled in the art will recognize that a mask that is used with a stepper is not formed on the substrate but is attached to the stepper and is displaced from the surface of the wafer (substrate) so that all chips on the wafer may be exposed by the same mask.

Next, the Examiner states that a resist film is formed on the first mask film and refers to col. 5, line 18. Line 18 refers to a photoresist applied to the insulating film 21 (not insulating film 19 as discussed above) to form a resist layer 22. Referring again to Fig. 2b, it can be seen that resist layer 22 is formed on interlayer insulating film 21 and not on insulating layer 19 nor on the first mask 23. The Examiner now states that the resist film serves as a mask during the etching process and refers to col. 5, lines 32-35. While we agree that the resist film can be considered a mask film, in sharp contrast to the "first mask" (not first mask film) 23, this does not fit in with formation of the other elements of the claim referred to above that the Examiner has maintained.

The Examiner states that furthermore Tsuji teaches the formation of a second mask film and refers to col. 5, line 46. Lines 45-46 recite "...the second exposure is carried out on the resist film 22 with use of a second mask 31 having a pattern..". The second mask 31 is shown in Figs. 3A and 3B. Again, this is not recited as a second mask film, only a second mask, which is again a reticle which is separated from the substrate and thus not formed on the substrate. The Examiner states that Tsuji teaches a formation of a wiring layer by burying an electroconductor material in the trenches. This is true, although it should be noted that two different types of trenches are formed, discussed below. The Examiner states Tsuji discloses that the second mask is located in the same position where the next opening would be later etched. Tsuji uses a reticle in a stepper. As is well known to those skilled in the art, the stepper is used to expose each chip using a plurality of masks to perform a plurality of processing steps. Thus, one would expect that the stepper will expose the chip to the next mask at the same location, as each chip would be exposed to all of the masks. The Examiner states that given the fact that the second opening in applicant's invention is etched through the sidewalls covered with the second mask film, it is the Examiner's position that Tsuji's disclosure about the position of the openings etched at the deposition of the second mask reads on applicant's limitation of "the second mask film covering sidewalls and the bottom of the trenches".

The only film formed by Tsuji which could meet the requirements of either the first or the second mask film of the present invention is the resist layer 22. In Tsuji, the resist layer is exposed twice but only etched once. After the first exposure using reticle 23, the resist undergoes a heat treatment in which the area of resist exposed to light is hardened in order to decrease the solution (etch) rate of that region, see col. 5, lines 28-36. Then, the same resist layer is exposed a second time but the portion exposed to light is not subjected to a heat treatment, and therefore the resist does not undergo the change in the etch rate (see col. 5, lines 39-43). Later, during the single etch process, the areas of resist that were exposed to the heat treatment are hardened to the alkali etch material and are not removed so that a contact hole or via is formed and the sidewalls remain. At the same time, the single etch of Tsuji dissolves the resist material that has not been hardened so that not only is a trench formed, but the sidewalls are

significantly etched down so that a wiring layer can be placed above the contact hole or via. Thus, the finished contact hole is shown in Fig. 9A and the finished contact hole with the metal interconnect is shown in Fig. 9B. Comparing Figs. 9A and 9B, we see that the sidewalls 21 are at full height in Fig. 9A, but have been reduced to approximately half height in the embodiment of Fig. 9B. Both of these structures can be formed at the same time using the Tsuji technique. There is no showing of the Examiner's second mask 31 on the sidewalls as required by the present claims.

In sharp contrast, the present invention utilizes two separate mask films which are formed on the substrate. We know that there are two separate mask films, because a portion of the first mask film is removed before the second the mask film is formed. This portion of the first mask film is removed during the first etching step which is followed by the formation of trenches in the insulating film exposed from the opening. The second mask film is then formed after which the horizontal surfaces thereof are removed leaving only the sidewall portions and a second etch is performed using the first mask film and the second mask film as the etching mask for etching the trenches deeper.

In summary, Tsuji shows a single mask film, resist 22, which is exposed twice and etched once whereas in the present invention two mask films are formed, each of which is exposed and etched separately. The purpose of Tsuji is to form the connecting holes or vias and connecting holes or vias with metal interconnects in the same series of steps. The purpose of the present invention is to produce a trench having a sharper vertical sidewalls than available in the prior art. In view of the fact that the masks of Tsuji are not on the substrate, they cannot protect against the processing problems described in our application at page 2, lines 3-15.

As stated in previous responses, it is very important to understand the difference between a "first mask" and a "first mask film". Although they sound very similar, the term, "first mask", as utilized in Tsuji, refers to the exposure mask which is mounted in the reticule on the stepper and used to expose the resist layer 22. In sharp contrast, the term "first mask film" as utilized in the present invention refers to a film which is formed on an insulating film which is in turn formed on the semiconductor substrate or SOI substrate. Note that the claims, such as Claim 1, recite "forming a first mask film on the insulating film", (emphasis added). It should also be noted that the present claims

require the second mask film on the sidewalls of the trenches, which is not shown or suggested by Tsuji.

One clue to the Examiner's misinterpretation of Tsuji is that the first mask 23 is recited at col. 5, lines 24-25, whereas the resist which is to be formed on the first mask film, according to the Examiner, resist layer 22, is recited at col. 5, lines 16-20. Thus, in Tsuji, the resist is formed before the Examiner's "first mask 23" making it impossible for the resist film to be formed on a first mask "film", as required by the present claims.

CONCLUSION

For the above reasons, Applicants respectfully submit that the Examiner's final rejection of Claims 1-10 under 35 U.S.C. 103(a) as being unpatentable over Tsuji in view of Harari is not properly founded in law. Applicants respectfully request that the Board of Patents Appeals and Interferences so find and reverse Examiner's rejections of the claims.

Please charge any fees in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 20-0668 of Texas Instruments Incorporated. **This form is submitted in triplicate.**

Respectfully submitted,



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APPENDIX

1. (Four Times Amended) A manufacturing method of a semiconductor IC device, comprising the following steps :

forming an insulating film on a semiconductor substrate or SOI substrate;

forming a first mask film on the insulating film;

forming a resist film on the first mask film, the resist film being used as an etching mask to form an opening on the first mask film, followed by the formation of trenches on the insulating film exposed from the opening

forming, after the resist film is removed, a second mask film on the semiconductor substrate or SOI substrate, said second mask film covering side walls and a bottom of the trenches;

removing the second mask film from the bottom of the trenches without removing the second mask film on the side walls of the trenches, forming a side wall made of the second mask film on the side walls of the trenches;

and using the first mask film and the second mask film as the etching mask in etching said trenches deeper than a thickness of said insulating film so as to penetrate into a portion of said substrate to form connecting holes.

2. (Four Times Amended) A manufacturing method of a semiconductor IC device comprising the following steps :

forming an insulating film on a semiconductor substrate or SOI substrate;

forming a first mask film on the insulating film;

forming a resist film on the first mask film, the resist film being used as an etching mask to form an opening on the first mask film, followed by the formation of trenches on the insulating film exposed from the opening

forming, after the resist film is removed, a second mask film on the semiconductor substrate or SOI substrate, said second mask film covering side walls and a bottom of the trenches;

removing the second mask film from the bottom of the trenches without removing the second mask film on the side walls of the trenches, forming a side wall made of the second mask film on the side walls of the trenches;

using the first mask film and the second mask film as the etching mask in etching said trenches deeper than a thickness of said insulating film so as to penetrate into a portion of said substrate to form an opening on the insulating film, followed by the formation of separating trenches on the semiconductor substrate or SOI substrate exposed from the opening;

burying an insulating film in the separating trenches to form a separating portion.

3. (Four Times Amended) A manufacturing method of a semiconductor IC device comprising the following steps :

forming an insulating film on a semiconductor substrate or SOI substrate;

forming a first mask film on the insulating film;

forming a resist film on the first mask film, the resist film being used as an etching mask to form an opening on the first mask film, followed by the formation of trenches on the insulating film exposed from the opening

forming, after the resist film is removed, a second mask film on the semiconductor substrate or SOI substrate, said second mask film covering side walls and a bottom of the trenches;

removing the second mask film from the bottom of the trenches without removing the second mask film on the side walls of the trenches, forming a side wall made of the second mask film on the side walls of the trenches;

and using the first mask film and the second mask film as the etching mask in etching said trenches deeper than a thickness of said insulating film so as to penetrate into a portion of said substrate to form wiring-forming trenches on the insulating film, followed by burying an electroconductive material in the wiring-forming trenches to form a wiring layer made of the electroconductive material.

4. (Amended) The manufacturing method described in Claim 1, wherein the insulating film is selected from the group consisting of a silica film, SOG film, PSG film, BPSG film, or a lamination consisting of these films, the first mask film and second mask film for the hook-shaped hard mask being selected from the group consisting of a

polysilicon film, tungsten film, or other electroconductive film, or a silicon nitride film or other insulating film.

5. (Amended) The manufacturing method of a semiconductor IC device described in Claim 1, wherein the connecting holes are in contact with the lower electrodes in the capacitors of the memory cells, with the capacitors being set for storing information on the bit lines.

6. (New) The manufacturing method of a semiconductor IC device described in Claim 4, wherein the connecting holes are in contact with the lower electrodes in the capacitors of the memory cells, with the capacitors being set for storing information on the bit lines.

7. (New) The manufacturing method described in Claim 2, wherein the insulating film is selected from the group consisting of a silica film, SOG film, PSG film, BPSG film, or a lamination consisting of these films, the first mask film and second mask film for hook-shaped hard mask being selected from the group consisting of a polysilicon film, tungsten film, or other electroconductive film, or a silicon nitride film or other insulating film.

8. (New) The manufacturing method of a semiconductor IC device described in Claim 7, wherein the connecting holes are in contact with the lower electrodes in the capacitors of the memory cells, with the capacitors being set for storing information on the bit lines.

9. (New) The manufacturing method described in Claim 3, wherein the insulating film is selected from the group consisting of a silica film, SOG film, PSG film, BPSG film, or a lamination consisting of these films, the first mask film and second mask film for hook-shaped hard mask being selected from the group consisting of a polysilicon film, tungsten film, or other electroconductive film, or a silicon nitride film or other insulating film.

10. (New) The manufacturing method of a semiconductor IC device described in Claim 9, wherein the connecting holes are in contact with the lower electrodes in the capacitors of the memory cells, with the capacitors being set for storing information on the bit lines.